Claim 1 (currently amended): A method for performing proximity effect correction on a layout of an integrated circuit defined by a computer readable layout file, to produce a corrected layout file, the method comprising:

receiving a polygon from the computer readable layout file, the polygon corresponding to a portion of the integrated circuit;

performing using a data processor a fragmentation of the polygon into a set of smaller shapes, based upon parameters of a manufacturing tool used for implementing the layout;

performing using a data processor a proximity effect correction of at least one of the smaller shapes in the set of smaller shapes to provide a computer readable corrected layout file comprising a modified set of smaller shapes, wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction;

and

providing the computer readable corrected layout file to said manufacturing tool.

Claim 2 (original): The method of claim 1, wherein the manufacturing tool comprises a mask writer.

Claim 3 (original): The method of claim 1, wherein the manufacturing tool comprises a vector scan, e-beam tool, and said parameters comprise scanning dimensions of said vector scan, e-beam tool.

Claim 4 (currently amended): The method of claim 1, wherein one of said parameters is a minimum dimension for the manufacturing tool, and the fragmentation is such that the smaller shapes do not have a dimension smaller than said minimum dimension after said proximity effect correction.

Claim 5 (currently amended): The method of claim 1, wherein one of said parameters is a maximum dimension for the manufacturing tool, and the fragmentation is such that the smaller shapes do not have a dimension larger than said maximum dimension after said proximity effect correction.

Claim 6 (original): The method of claim 1, wherein the corrected layout file is used to make a binary mask.

Claim 7 (original): The method of claim 1, wherein the corrected layout file is used to make an attenuated phase-shifting mask.

Claim 8 (original): The method of claim 1, wherein the corrected layout file is used to make a tri-tone phase-shifting mask.

Claim 9 (original): The method of claim 1, wherein the corrected layout file is used to make an alternating aperture

phase-shifting mask.

Claim 10 (original): The method of claim 9, wherein two edges of one of the shapes in the set of smaller shapes are adjacent to two distinct phase-shifting regions, the two phase-shifting regions are substantially out of phase, and including storing information indicating that said two edges of one of the shapes in the set of smaller shapes are adjacent to two distinct phase-shifting regions.

Claim 11 (original): The method of claim 10, wherein said information about the two edges is used to facilitate the phase assignment of the phase-shifting regions.

Claim 12 (original): The method of claim 1, wherein at least one edge of one shape abuts a boundary of a critical area of the layout.

Claim 13 (original): The method of claim 1, wherein the manufacturing tool comprises a mask inspection tool.

Claim 14 (canceled).

Claim 15 (original): The method of claim 1, wherein a second polygon within proximity range of the polygon is taken into account in the fragmentation of the shapes.

Claim 16 (original): The method of claim 15, wherein a corner of the second polygon is used in the fragmentation of the shapes.

Claim 17 (canceled).

Claim 18 (currently amended): A method for manufacturing integrated circuits, said integrated circuits being defined by a computer readable layout file, the method comprising:

receiving a polygon from the computer readable layout file, the polygon corresponding to a portion of the integrated circuit;

performing using a data processor a fragmentation of the polygon into a set of smaller shapes, based upon parameters of a manufacturing tool used for implementing the layout;

performing using a data processor a proximity effect correction of at least one of the smaller shapes in the set of smaller shapes to provide a computer readable corrected layout file comprising a modified set of smaller shapes, wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction;

~~and~~

providing the computer readable corrected layout file to said manufacturing tool;~~,~~

producing a mask having a mask layout based on the corrected layout file;

and

exposing a semiconductor treated with a material sensitive to radiation energy to said radiation energy using said mask.

Claim 19 (currently amended): The method of claim 18, wherein ~~where~~ the mask is produced using a vector scan, ~~vector-scan~~ e-beam tool by exposing a mask blank coated with an e-beam sensitive resist and said resist polarity is chosen such that the shapes representing the critical dimensions of the layout are exposed on the mask.

Claim 20 (currently amended): A method for producing a mask for a layer on an integrated circuit represented by a computer readable layout file, comprising:

receiving a polygon from the computer readable layout file, the polygon corresponding to a portion of the integrated circuit;

performing using a data processor a fragmentation of the polygon into a set of smaller shapes, based upon parameters of a manufacturing tool used for implementing the layout;

performing using a data processor a proximity effect correction of at least one of the smaller shapes in the set of smaller shapes to provide a computer readable corrected layout file comprising a modified set of smaller shapes, wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction;

and

producing a mask having a mask layout based on the corrected

layout file.

Claim 21 (currently amended): A system for producing layout data, comprising:

a data processor which executes programs of instruction;

memory accessible by the data processor and storing programs of instruction, the programs of instruction including logic to receive a polygon of a computer readable layout file of a portion of the integrated circuit, performing using a data processor a fragmentation of the polygon into a set of smaller shapes, based upon parameters of a manufacturing tool used for implementing the layout, performing using a data processor a proximity effect correction of at least one of the smaller shapes in the set of smaller shapes to provide a computer readable corrected layout file comprising a modified set of smaller shapes, wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction.

Claim 22 (currently amended): An article of manufacture, comprising a machine readable data storage medium storing programs of instruction, including logic to receive a polygon of a computer readable layout file of a portion of the integrated circuit, performing using a data processor a fragmentation of the polygon into a set of smaller shapes, based upon parameters of a

manufacturing tool used for implementing the layout, performing using a data processor a proximity effect correction of at least one of the smaller shapes in the set of smaller shapes to provide a computer readable corrected layout file comprising a modified set of smaller shapes, wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction.

Claims 23-25 (canceled).